CLAIMS

1. The method for manufacturing and testing semiconductor components comprising the steps of:

providing a plurality of semiconductor devices;

providing a device carrier, said carrier having interconnect wiring therein sufficient for both testing and end use operation of said semiconductor devices;

attaching said semiconductor devices to said carrier;

testing said devices via said wiring; and

dividing said carrier into a plurality of components wherein each said component contains at least one said semiconductor device.

2. The method according to claim 1, further comprising the step of installing one said component on a next level of assembly without separating said device from said carrier.

3. The method according to claim 1, further comprising the step of installing one said component in an information handling system without separating said device from said carrier.

4. The method according to claim 1, wherein said carrier comprises a printed circuit board or a flex.

5. The method according to claim 1, wherein each of said semiconductor devices comprises a plurality of leads and wherein said carrier comprises contacts for external connection, the method further comprising the step of providing a lead reduction mechanism on said carrier, said lead reduction mechanism connected to said carrier contacts.

6. The method according to claim 5, wherein said lead reduction mechanism comprises a built-in self-test engine.

7. The method according to claim 6, wherein each semiconductor device comprises one said built-in self-test engine.

8. The method according to claim 7, wherein said built-in self-test engine includes less than ten external contacts for controlling said test engine, and wherein said semiconductor devices are connected in parallel to said external contacts for test or burn-in.

9. The method according to claim 7, wherein said semiconductor devices are organized in a plurality of groups on said carrier wherein BIST pads on said devices in each group are connected in parallel to separate external contacts.

10. The method according to claim 9, further comprising the step of burning-in or testing groups of devices in parallel with a separate BIST reader for each group.

11. The method according to claim 6, further comprising the step of testing or burning in said semiconductor devices using said built-in test engine.

12. The method according to claim 11, further comprising the step of separating said built-in self test engine from said carrier.

13. The method according to claim 1, wherein said testing step comprises running said semiconductor devices simultaneously and independently of each other.

14. The method according to claim 1, wherein said lead reduction mechanism comprises connecting like leads of said plurality of semiconductor devices in common.

15. The method according to claim 1, wherein the method comprises dividing said carrier into separate multi-chip final assemblies.

16. The method according to claim 15, wherein said multi-chip assemblies comprises single-in-line multi-chip modules or dual-in-line multi-chip modules.

17. The method according to claim 1, further comprising the step of mounting said semiconductor component on a second carrier.

18. The method according to claim 17, wherein said carrier comprises a flex, and wherein said second carrier comprises a printed circuit board, a second flex, a ceramic substrate, or a semiconductor substrate.

19. The method according to claim 18, wherein said flex comprises leads, said method further comprising separating adjacent leads from each other to facilitate connection to said second carrier.

20. The method according to claim 18, wherein a plurality of said components are connected to said second carrier to form an interconnected stack.

21. The method according to claim 1, wherein said carrier comprises connectors for connecting semiconductor devices on two sides of said carrier.

22. The method according to claim 1, further comprising the step of encapsulating said semiconductor devices and said carrier in an encapsulant.

23. The method according to claim 1, further comprising the step of identifying defective semiconductor devices.

24. The method according to claim 23, further comprising the step of invoking redundancy to repair said defective devices.

25. The method according to claim 23, further comprising the step of removing and replacing said defective semiconductor devices with replacement semiconductor devices.

26. The method according to claim 25, further comprising the step of repeating said

testing, identifying, and removing and replacing until no defective semiconductor devices are identified.

27. The method according to claim 25, wherein said replacement semiconductor devices have passed testing and burning-in on another carrier so no further burning-in is required.

28. The method according to claim 1, wherein said semiconductor devices are memory chips, the method further comprising testing said memory chips at speed.

29. The method according to claim 1, wherein said testing comprises testing functionality, testing for sensitivities, or testing fuses.

30. A semiconductor structure comprising:

a device carrier, said carrier having interconnect wiring therein sufficient for both testing and end use operation of said semiconductor devices;

a plurality of semiconductor devices mounted to said carrier; and

wherein said devices on said carrier may be tested and burned-in and wherein said carrier may be divided into a plurality of components, and wherein said components may be installed in an information handling system without separating said devices from said carrier.

31. The semiconductor structure of claim 30 wherein said carrier comprises contacts for external connection, said structure further comprising a lead reduction mechanism on said carrier, said lead reduction mechanism connected to said contacts of said carrier.

32. A semiconductor structure comprising:

a stack of flex device carriers, at least one semiconductor device mounted to each said flex carrier; and

an interconnect substrate, wherein said flex device carriers are electrically connected to said interconnect substrate.